2013 ECTC Special Forum

Commercializing TSV 3DIC Wafer Process Technology Solutions for Next Generation of Mobile Electronic Systems

Herb Huang, Ph.D. and Sudipto Roy, Ph.D.

Semiconductor Manufacturing International Corporation

May 28, 2013

Outline

- System & Device Levels: Driving Forces for 3DIC
- Status of Technology Readiness for TSV 3DIC along the Supply Chain
- TSV-based 3DIC SiP for Handheld to Wearable
- Outweighing Controlling Factors in Solutions & Evolution
- Collaborative Supply-Chain 3DIC Foundry Model
- Closing Remarks

Electronic System, IC Packaging & Device Evolution

Dominant Systems

IBM "ENIAC" Computer

PC Era

Palm

2G/3G MP

Smartphone

Smart -glass

Smart-watch

Laptop

Tablets

Ultra-book

1G MP DynaTAc

Packaging Formats

Discrete PKG

DIP PKG

FC-BGA

MAP- POP

FC-POP

3DIC

3DSiP

2.5DSiP

TSOP

BGA

MCM BGA

PoP

Si Devices & IC

1st Transistor

1st CPU ~um

1st Bipolar

1st IC

1st CMOS

Pentium 4

32nm CPU (HKMG)

A6 APU

Quantum Devices?

MeFET?

20nm FinFET

1950 1970 1990 2000 2010 2020

Smart Phone-Tablet-Wearable: Core Features & Enablers

Core Functions			 
Communication	• Multi band 2.5/3G/LTE wireless FE & baseband	• Multi band 2.5/3G/LTE wireless FE & baseband	• Multi band 2.5/3G/LTE wireless FE & baseband
Computing	• ARM core APU • GPU	• Multicore low power APU or LP CPU • GPU	•ARM core APU • GPU
Connectivity	• Bluetooth, WiFi • GPS, FM	• Bluetooth, WiFi • GPS, FM	•Bluetooth, WiFi •GPS, FM •Other low power NFC?
Display & interaction	• High Res, touch sense Integrated display • Controller/interface	• Highest Res, touch sense Integrated display • Fast controller/interface	• Projection, bright & mini display • Voice control interface
Battery & power management	• Thin high capacity battery • PMU supporting all IC	• Thin, highest capacity battery • PMU supporting all IC	• Compact high capacity battery • 1 PMU mini overall power
Imaging & sensing	• High Res & video CIS • 10-degree motion sensing • Multi noise cancelling mic	• High Res & video CIS • 10-degree motion sensing • Multi noise cancelling mic	• Ultra compact camera • 10-degree motion sensing • Mini N/S cancelling mic's
Key enabling factors for all overall functions	• Acceptable cost •Thin format •High performance (inc LP)	• High performance • Acceptable cost • Thin format	• Ultra small, thin • Ultra low power • Acceptable cost

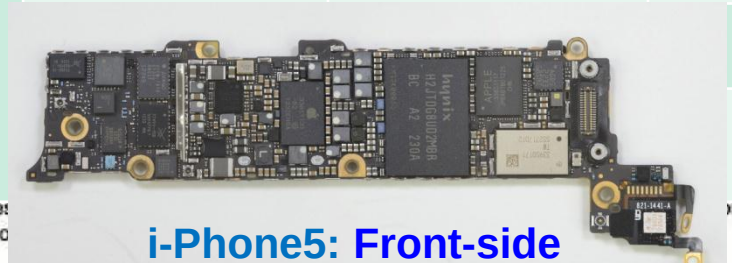
Evolution of IC & Electronic System Integration

	Now	Future	Additional Technology Requirements	TSV 3DIC: Pro & Con
Dominant Driving of Systems	Smartphone Tablet	e-Wearable's: Smart-watch Smart-glass	• Thinner, lighter, smaller • Low power, high speed • Connectivity, computing, interactivity • Flat or lower costs	•++ •++ •--
Trend: IC & Subsystem Packaging	PoP, MCM, Discrete on PCB	More "3D"SiP on PCB, less discrete & isolated MCM	•Higher, denser I/O pins •More RDL layers in SiP •Thinner, smaller format •Hybrid stack integration •Lower cost, •Better reliability	•++ •++ •++ •++ •-- •+
IC Devices & Fabrication	HKMG to FinFET	FinFET bulk Si, SOI	•Better device variation management •Decouple logic with MS/RF to 2 chips, maybe at different nodes or technologies	•++ •++

Example: Chips to SiP Grouping on Smartphone PCB

Front Side	MCP/ SiP	TSV SiP Option	Back Side	MCP/ SiP	TSV Option
WiFi module	WiFi FEM SiP	Maybe but costly	**APU**	DRAM MCP	TSV Wide I/O best option but costly & manufacturability
3-axis gyroscope	MEMS+ASIC SiP	TSV SiP: thinner, better noise isolation Combo SiP: Single chip	**LTE Baseband Processor**	PMIC on front-side connected through PCB	Split logic potion with MS/RF to two chips, 2.5D SiP
3-axis accelerometer	MEMS+ASIC SiP		**Audio Chips**	Analog MCP	May stay separated for noise isolation
Touch screen controller.	Interface	Performance gain but costly	**Imaging Sensor Camera Module**	13M BSI	Can further thinner WL camera module
PA GSM/GPRS/EDGE	SiP with matching switches, IPD, LNA	TSV SiP for PA module: improving noise performance, but cost needs justification	**Microphones**	3 in different packages & sites	No help
CDMA Power Amplifier					
PA					
PA LTE					
PA					
PA WCDMA / HSUPA					

i-Phone 5: Back-side

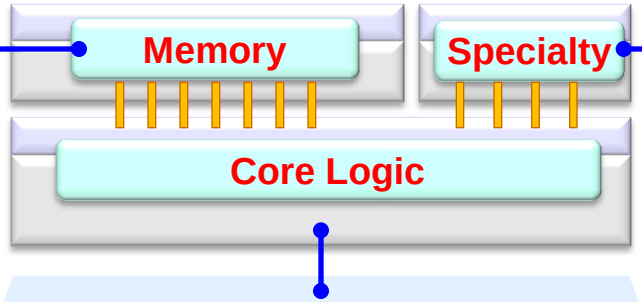


i-Phone5: Front-side

SMIC

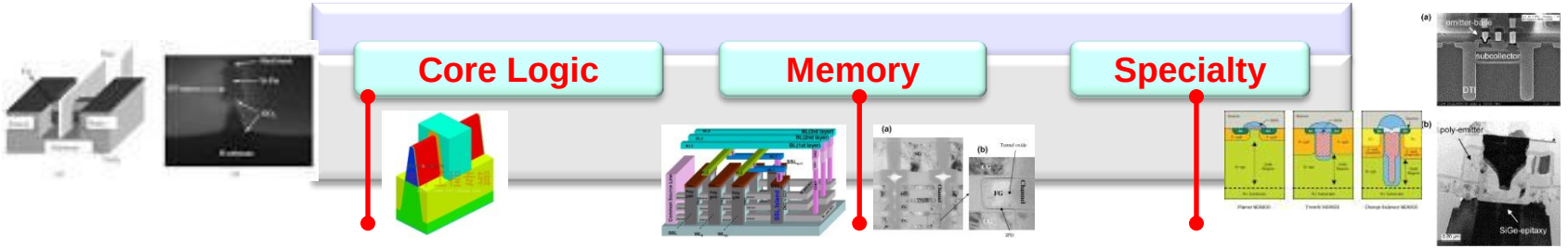
Device Level: Alternative "Process Integration"

Dedicated memory MOS
Better fine pitch dense array & OPC
Optimized implants & thermal budget



Dedicated specialty MOS
Gross litho CD & variable patterns
Specialized implants & analog tuning

Enhanced, dedicated CMOS (FinFET) design
Better ultra fine CD & OPC control
Simplified baseline implants & thermal budget



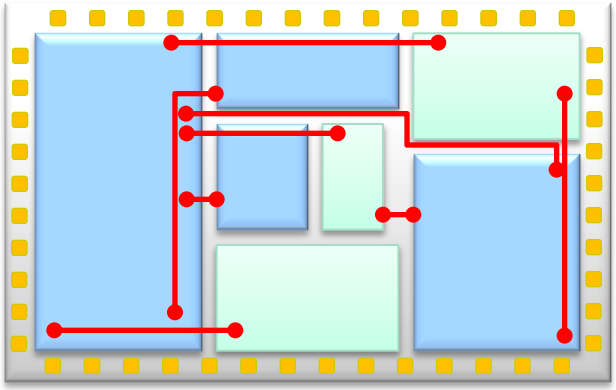
HS/LP dominant (to FinFET)
Ultra fine CD, fine array
Baseline implants & constrained thermal budget

2 Poly Cell
Fine pitch stacked array
Special implants & thermal budget (to emerging NVM)

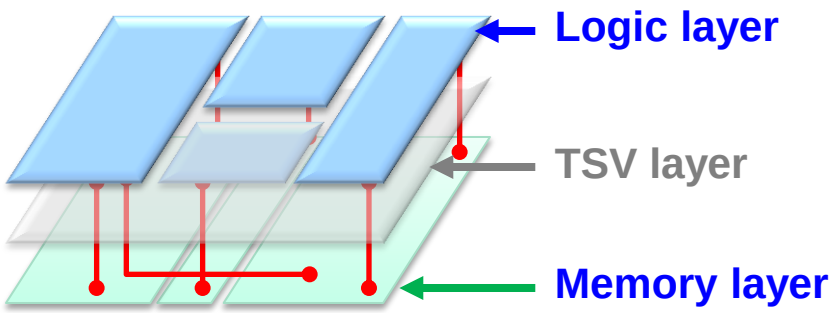
Specialty & even analog MOS
Variable CD & patterns
Special implants & analog performance

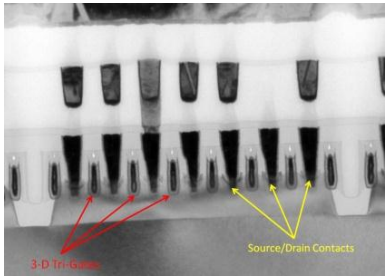
Chip Level: Alternative "Interconnect" to 2D SOC

2D homogenous SOC



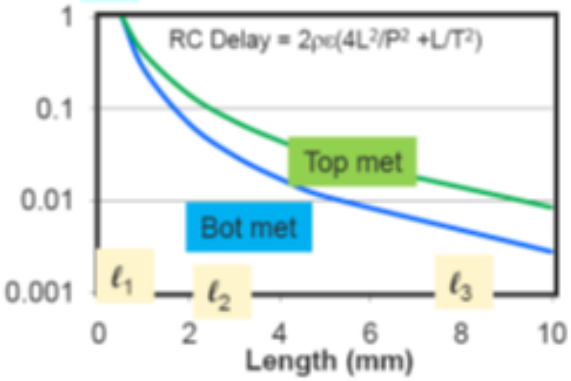
3D reconfigured architecture





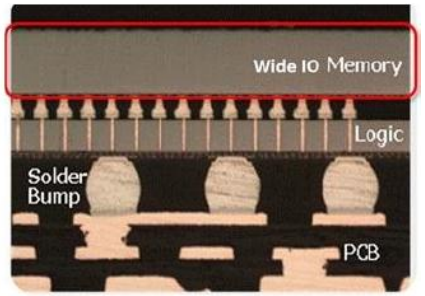
2D SOC

- Die size ↑
- MT X-sec ↓
- MT length ↑
- RC delay ↑
- Power ↑



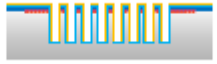
TSV 3D

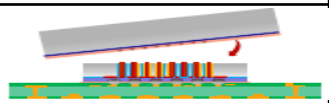
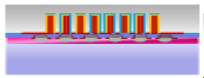
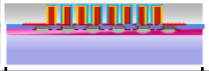
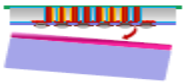
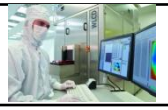
- ↓ Die size
- ↑ MT X-sec
- ↓ MT length
- ↓ RC delay
- ↓ Power



1. FEOL CD => ~10nm, BEOL CD ~10's nm; narrowing long on-chip interconnects
2. Advance in IMD (LK => ELK) ceases, limiting further RC reduction

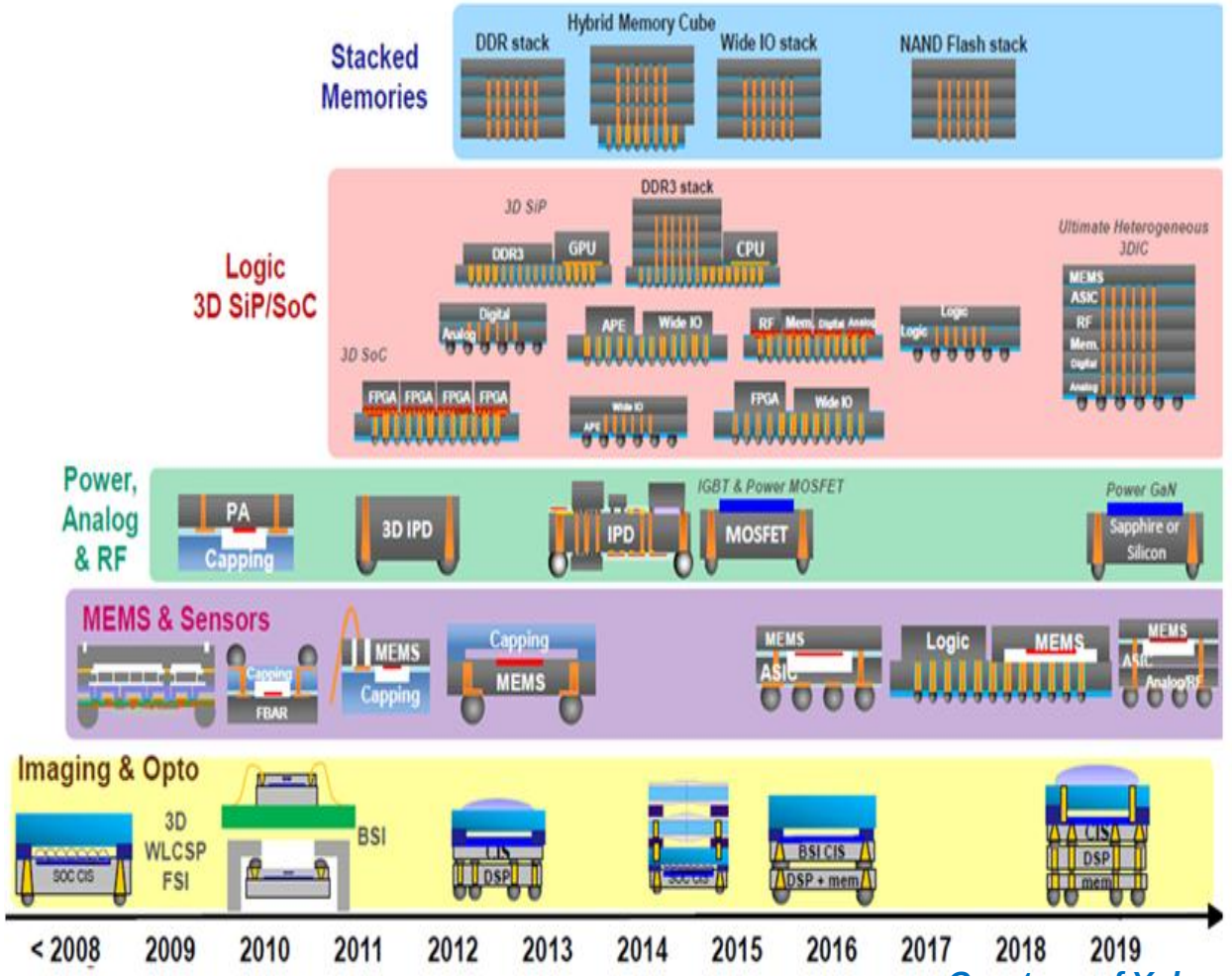
Readiness: Supply Chain Manufacturability Today

Via-Mid Front-end	TSV-mid litho	TSV-mid etching	TSV-mid isolation	Barrier/seed DEP	TSV ECP	Post ECP Cu CMP	BEOL/FS-RDL/Bump
Foundry process							
Capability vs. spec							
Window & CDU							
Tool maturity							
Running cost & throughput	Acceptable for risk run	Ready for pilot	Mature 4 mass production	Close to acceptable			

Via-Mid Middle-end	Stacking & Bonding			Temp bond to carrier	Thinning /grinding	TSV reveal	Carrier debonding	Inspect & metrology	WL & SiP Testing
OSAT Process									
	CtC	CtW	WtW						
Capability vs. spec									
Window & CDU									
Tool maturity		Engineering run							
Running cost & throughput		Not ready							

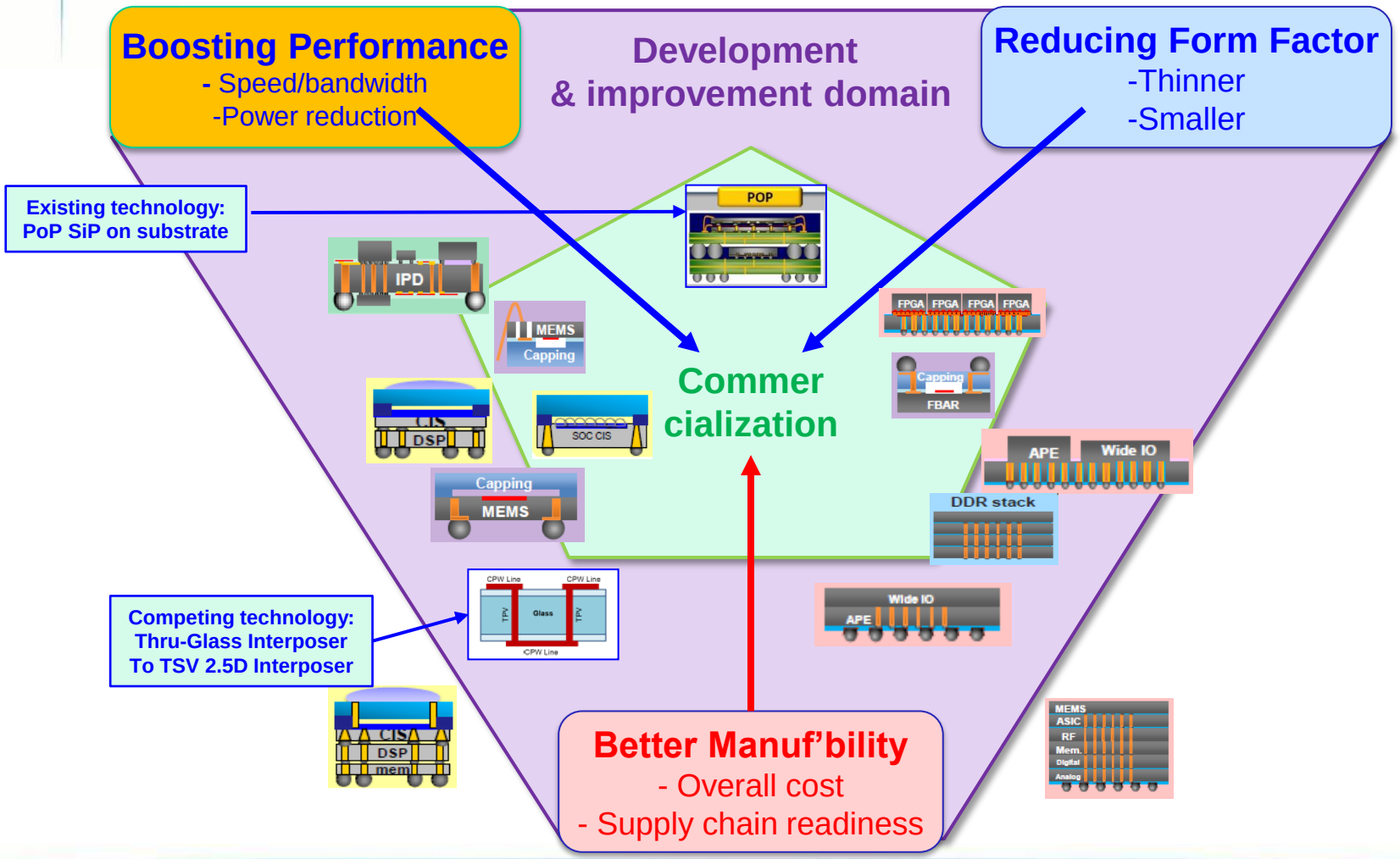
TSV 3DIC Implementation Roadmap: Pro & Con

Key Pro Factors	Key Con Factors
• Data speed • PKG thickness	•KGD •Cost •Yield
• Speed • PKG thickness • Wafer process	• TSV-CMOS • I/O interface • Cost • Yield
• Noise isolation • PKG thickness	• Cost (unless performance justified)
•PKG thickness •Noise isolation • Cost reduction thru WLP	• Technical feasibility
• PKG thickness • Functional requirements • Cost reduction thru WLP	• Difficult for large format chips



Courtesy of Yole

3DIC Commercialization: Key Factor Paradigm



3DIC for Overall Cost Reduction: Practical Solutions

Conventional fabrication & assembly constructions

- BGA
- Frame-based connects
- DtD & DtW CtS wire bonding
- WL thick film/bumping
- PoP
- Wafer level thin film process
- DtD & DtW flip chip connects
- Chip to board assembly

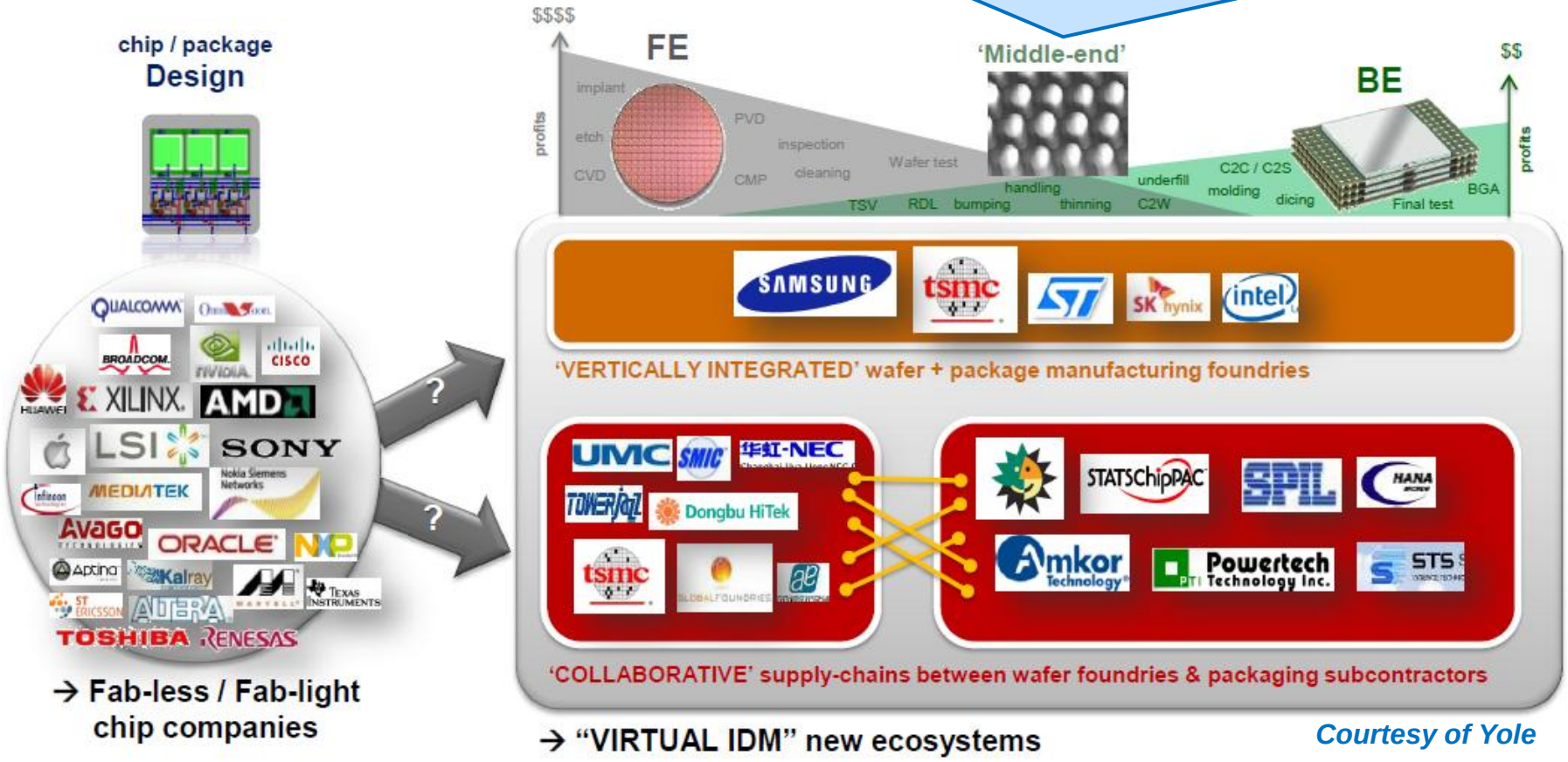
Multilayer Substrate Board (with thru-board Via)

Intro TSV	CMOS & local interconnects	On-chip global interconnects	Inter-chip interconnects	Chips to PKG Carrier Connects	PKG I/O Connects (to Board)
TSV -based 2.5D SiP	Wafer FE + bumping	TSV Si interposer	Die to TSI flip chip	DtS flip chip / DtS wire bond	To substrate board assembly
Wide I/O TSV 3D SiP	CMOS FEOL + TSV + BEOL + bumping		Die to Die flip chip	DtS flip chip / DtS wire bond	Board assembly

Innovative re-constructions needed for overall cost reduction
Economically viable solution is in sight

Emerging Mid-End & Two Ecosystem Models

- Technical spec (DR, etc) & hands-off: must shared from FE, ME, BE to system
- Productization & commercialization: only verified along full line down to system level
- Foundry & OSAT: best to leverage existing, differentiating but matching core strength & capability over ME, extended from FE and BE respectively



Courtesy of Yole

Collaborative & Full 3DIC Foundry Services

Key Competency & Services	IC Design	Devices on Wafer Fab & WL Testing	Wafer Level Packaging	Chip to System Packaging &Testing	System & Board Assembly	(Sub) System Design & Application
IDM's Or wafer +WLP+P&T	Complete vertical integration; Full foundry model; Ext Service Or sub con					
Fab-lite & fabless	Core Value & Strength; Extended engineering design for sub con					
CMOS Wafer Foundry	Design Service; Core Value & Strength; TSV Via-mid					
WLP Partner			Ext Serv; Core Value & Strength			
Chip & SiP & Testing Partner	Collaborative 3DIC Foundry Model		Expanded service; Core Value & Strength; Ext Service			
System Assembler & User					Core Value & Strength; Ext Service	

- Extra Capex $
- New, diff OPS
- Limited capacity
- High MFG $

Closing Remarks

System towards mobile wearable driving supply chain to TSV 3DIC development & commercialization

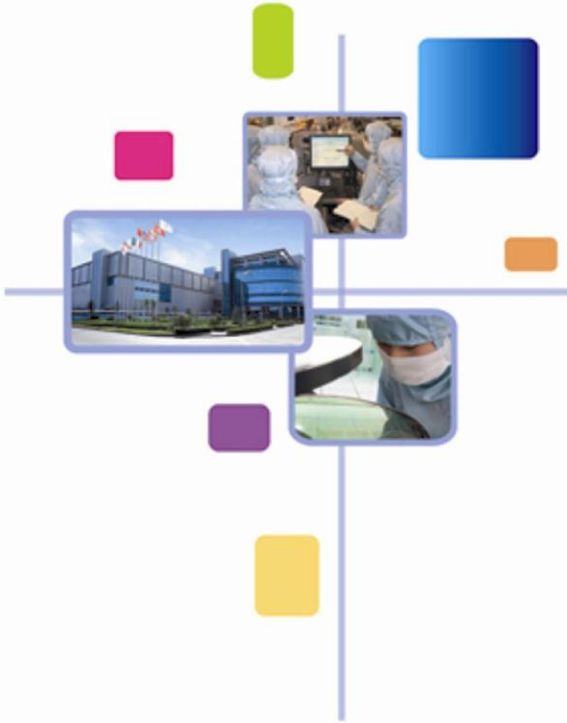
- Mobile, handheld to wearable are inevitable, and a dominant trend
- Main electronic boards forced to shrink in size and thickness
- Core & peripheral chips continue to regroup to smaller, thinner SiP; isolated functional chips thinner, smaller; discrete devices to consolidate into SiP or SoC

Miniaturization, performance boost and overall manufacturing cost: tri-driving and limiting factors in paradigm of commercialization

- Scenario 1: performance gain outweigh increase in overall cost
- Scenario 2: 3D WLP and miniaturization also reducing overall cost
- Scenario 3: ultra thin becomes must for system & SiP integration

Collaborative TSV 3DIC foundry service: an adequate model to address overall supply chain manufacturability & costs

- Leverage available development resources, manufacturing lines, minimize overall capital investment and running costs
- Sustain & growth supply-chain ecosystem in collaborative evolution



Thank You

Semiconductor Manufacturing International Corporation

SMIC

Q&A